Abstracts

A low jitter 5.3-GHz 0.18-/spl mu/m CMOS PLL based frequency synthesizer

S. Ali and F. Jain. "A low jitter 5.3-GHz 0.18-/spl mu/m CMOS PLL based frequency synthesizer." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 173-176.

A 5.3-GHz CMOS phase locked loop (PLL) based frequency synthesizer is reported. The PLL operates as an integer-N frequency synthesizer using a ring-type voltage controlled oscillator (VCO). The PLL based synthesizer operates from 4.9 to 5.3-GHz and achieves a phase noise of -121.9 dBc/Hz at 10-MHz offset frequency from the carrier for maximum oscillation frequency of 5.3-GHz. The ring VCO works from 4.21 to 5.46-GHz with a maximum power consumption of 4.7-mW. A completely ripple-free VCO control voltage is obtained using a current mirror current source in a charge pump loop filter. The PLL is implemented with TSMC 0.18-/spl mu/m technology for GSM applications. The output rms jitter is 0.3% of the oscillator period. The total power consumption of this synthesizer is only 10-mW from a 1.8 V power supply.

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